ABSTRACT OF THE DISCLOSURE

A reference cell is connected to two reference bit lines. In data access, when one reference bit line is driven to a selected state in response to a reference column select signal which is a decode result of a column address, a potential of a selected reference bit line is transmitted to a reference data bus line. A potential difference between the reference data bus line and a data bus line is amplified by a sense amplifier, and read data is output from an external terminal. During the access period, a reference bit line in a non-selected state is precharged to a ground potential in response to a reset signal at H level. In the next data access, when the non-selected reference bit line is selected, successive data reading is attained without waiting for a time period for precharging a bit line.